EEE174 –CpE185 Introduction to Microprocessors

LAB 5 – PLC

**Lab Session: Wednesday 6:30PM - 9:10PM**

**Section 32385**

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Table of Contents

[Part 1 3](#_Toc508793889)

[Overview 3](#_Toc508793890)

[Lab Discussion 4](#_Toc508793891)

[Work Performed / Solution: 4](#_Toc508793892)

[Listing Files(s): 5](#_Toc508793893)

[Conclusion 6](#_Toc508793894)

# Part 1

## Overview

This lab is a short dive into the idea of the PLC or programmable logic controller. The idea with PLC’s is to be a simple, super reliable digital computer responsible for many industrial requirements. They are widely used due to their ease of use, reliability, and straight forward troubleshooting.

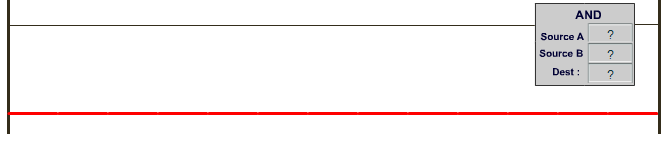
## Lab Discussion

### Work Performed / Solution:

First, an account needed to be created at the website provided under listing files for simulation. Once this account is created, we are then provided with a blank slate and many symbols available to place from the upper left hand corner. The website itself isn’t too intuitive at first so there is a video provided to watch under listing files. After watching the video I was still a bit confused due to the lack of audio in the video to explain what they were doing but gave it a shot anyway. I proceeded to add the instruction for add under the logic tab in the upper left hand corner:



After adding it to a rung it then looked like this and I had no idea what to do with it:



After fiddling with it trying to figure out what the input and output names should be I asked a nearby classmate that already completed it and received a much better explanation than the video.

The correct area to use is actually “basics” not “logic”. From here, we can then add different pieces of ladder logic to work as gates. There are breaks that need to be connected that when placed in series create an AND gate:



Here, unless both breaks in the line are connected, signal will not come through – like an AND gate. (Please see listing files for the truth tables of all the gates explored).



Now, there is an alternate path for the signal to flow so the only time signal will not flow is if both paths are not connected – just like an OR gate.



The second part to the logic equation is the output. Above is the symbol for normal output, where signal high is output as signal high and signal low is output in a similar fashion. Using this symbol inverts your output:



So combining this idea with the first two logics allow for NOR and NAND gates to be created since their truth tables are just the inverse of their NOT counterparts OR and AND respectively.

Using these ideas I designed a simple industry model for the operation of some sort of power plant. The idea is to have a plant than needs to have one or more operation managers on board at all times as well as a power delivery method and a monitoring / regulation method in order to be operational. If there is no manager or one of the delivery or monitoring solutions is not available then the plant does not run.

Implementing this idea, the left most portion will be 4 operations managers in an OR configuration and two breaks in an AND configuration for the monitoring and delivery solutions:

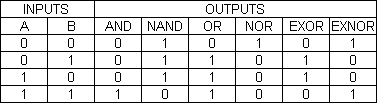


### Listing Files(s):

Provided website used for PLC simulation: <http://www.plcsimulator.net/>

Provided website used for learning PLC sim: <http://www.plcsimulator.net/help/ldsimulator.html>

Truth table courtesy of <http://www.ee.surrey.ac.uk/Projects/CAL/digital-logic/gatesfunc/> :



## Conclusion

The idea for this lab is really simple, I think the only improvement that could be made is a bit more clarity on the way the simulator we use works. In retrospect, I could have also looked up another YouTube video or even used a different simulator but this one does work. The idea behind a PLC is definitely “ruggedized”, as our lab describes. The concept is very easy to understand after to get what the symbols mean. I simply thought of a signal trying to get through lines and if the breaks would allow it or not.